A Low Spurious CMOS Image Sensor with a 4-input Comparator and a Hybrid Column Calibration Technique

Hyejin Im and Minkyu Song

***Abstract*—** In this paper, a low spurious CMOS Image Sensor (CIS) based on a 4-input comparator and a hybrid self-calibrated column technique is proposed. Conventionally, the operating speed of a two-step single-slope ADC is faster by about 10 times than that of a single-slope ADC. However, it has a serious connection error between the coarse block and the fine block. Thus a new 4-input comparator is proposed in order to improve the drawbacks of two-step single-slope ADC. Further, a self-calibrated column technique to adopt both an analog calibration block and a digital calibration block is also discussed. With a Samsung 0.13μm CIS technology, a test chip with the proposed techniques has been fabricated. The measured power consumption is about 98uW per column with the high frame rate of 120 frames/s (fps) at the VGA resolution. The measured pixel fixed pattern noise is about 0.43LSB which is much lower than the other conventional techniques.*

***Keywords*—**a low spurious CMOS image sensor, a 4-input comparator, a hybrid self-calibrated column technique, single-slope ADC, pixel fixed pattern noise

I. Introduction

Currently, the CMOS Image Sensor (CIS) has been very widely used including the digital camera, digital camcorder, CCTV and medical equipment and the research development in upgrading the frames are considered important due to the features in the rapid operation of the CIS. One of the major causes which degrade the image quality in the CIS is the low frame rate. It is determined by the conversion speed of the Analog to Digital Converter (ADC) existed in every column. Currently, the CIS used in various fields including the digital camera, digital camcorder, CCTV, medical equipment and vehicle system introduces the Single Slope ADC (SS ADC) with simple structure and excellent conversion performance [1]. However, the disadvantage exists that the conversion speed of the SS ADC becomes slow with 2^n times in proportion to increasing the resolution (n) and this makes it difficult to introduce to the system with high resolution including digital camcorder, HDTV or UDTV or the image sensor in the video area which requires high frame rates larger than 30 frames/s. Therefore, there have been studies on the Two-Step Single Slope ADC (TS SS ADC) with the conversion speed faster than the SS ADC by more than 10 times and similar area and power consumption [2][3]. However, due to the features of the TS SS ADC where the A/D conversion occurs in the upper (n-f) bit (coarse bit) and the lower (f) bit (fine bit), the Column Fixed Pattern Noise (CFPN) in proportion to the error in the slope ratio between the coarse ramp and the fine ramp is the main cause which degrades the image quality. Therefore, to eliminate the CFPN in the TS SS ADC CIS, the paper proposes the CMOS image sensor with 14-bit Two Step Single Slope ADC using the self-calibration technique.

II. CIS Architecture

Generally, the CIS with the column structure consists of the pixel array, analog Correlated Double Sampling (CDS) block and digital control block. The pixel array converts the light to the voltage and the voltage handled in the pixel to the digital signal through the column ADC. The digital control block plays a role in controlling the pixel, column and output interface. Fig.1 shows the architecture of the CIS which implements the 14-bit TS SS ADC and the column self-calibration technique. The CIS designed by this paper is based on the column-parallel structure, configured with the pixel array with the resolution of the VGA (640x480) and the pixel uses the 4-TR APS with the size of 5.6μm x 5.6μm. The column TS SS ADC consists of both one counter with the parallel load corresponding to the lower bit and two memories which store the digital values of the upper and lower bit. Further, it is designed with a memory for the self-calibration.

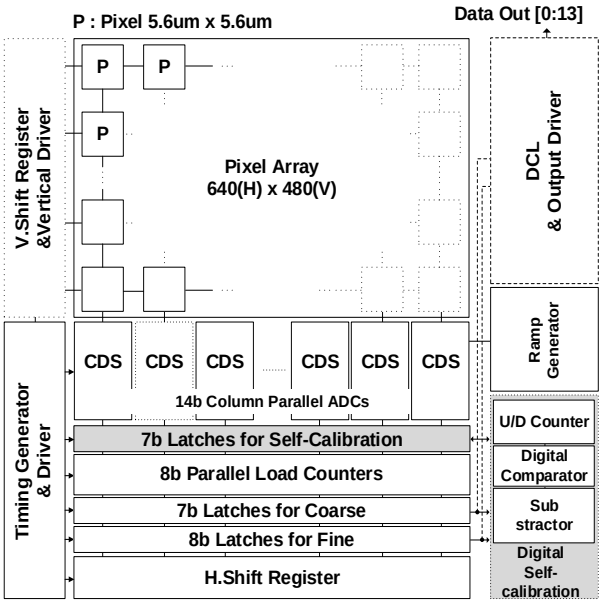


Fig. 1. Architecture of the proposed CMOS Image Sensor

Hyejin Im, Master Course , Dept. of Semiconductor Science, Dongguk University, South Korea

Minkyu Song, Professor, Dept. of Semiconductor Science, Dongguk University, South Korea,

https://doi.org/10.17758/EIRAI2.F0418109

III. CIRCUIT IMPLEMENTATION

A. *Two-step Single-slope ADC*

The proposed structure of the TS SS ADC is shown in Fig.2. The TS SS ADC structure proposed in this paper uses the 4-input comparator based on the gilbert cell mixer structure. As shown in Fig.2, the analog CDS block using the 4-input comparator performs the A/D conversion by applying different input for the coarse ramp and the fine ramp. Fig.3 shows the timing diagram for coarse bit A/D and the fine bit A/D conversion of the 4-input comparator. In this way, the proposed TS SS ADC can implement a two-step operation procedure as shown in Fig.2. This procedure is equal to conventional TS SS ADC. The advantages of proposed TS SS ADC are as follows. First of all, the input stage of the proposed TS SS ADC is very simple by using 4-input comparator. As a result, SADC1 and SADC2 switches of conventional TS SS ADC is eliminated, therefore switching noises are reduced by 1/3. Furthermore, the offset errors aren't generated because a V_{ref} is transferred to comparator continuously. And the biggest advantage of proposed TS SS ADC is an elimination of serial capacitor. For this reason, the fine ramp slope variation is not generated. In the proposed architecture, the holding capacitor is only used to hold on a coarse ramp. Thus, the fine ramp slope is not affected by the parasitic capacitor. Furthermore, coupling noise factors can be reduced. The Table I is a comparison table of 10-bit conventional TS SS ADC and a proposed 10-bit TS SS ADC performance. In simulation the proposed TS SS ADC has reduced noise factors in comparison with the conventional approach.

B. *Design of the self-calibration circuit*

As mentioned before, the difference in the slope ratio between the coarse ramp and the fine ramp creates the CFPN which degrades the image quality. To complement such problem, this paper proposes the analog CDS structure which uses the new 4-input comparator. Such structural change may sufficiently complement the slope changes in the ramp signal inside the comparator. However, the analog gain error of the ramp in the comparator may not be complemented by the structural changes in the analog CDS. Therefore, the circuit is required for the calibration. This paper proposes a circuit to correct the analog gain error in such comparator. Fig.4 (a) shows the circuit diagram of the 4-input comparator used in the proposed analog CDS structure. Here, the current in the M_{Coarse} and the M_{Fine} is not the same due to the mismatching of the two MOSs, causing to have uneven analog gain between the coarse ramp and the fine ramp and to have the difference in the slope ratio between the two ramps. Therefore, the study configures the analog calibration block to the M_{Fine} location which may change the gm value by adjusting the current amount on M_{Fine} to make the analog gain same in the M_{Coarse} and the M_{Fine}. Fig.4 (b) shows the analog calibration block circuit. The gm value in the M_{Fine} may be adjusted by trim SRAM signal in the digital calibration block.

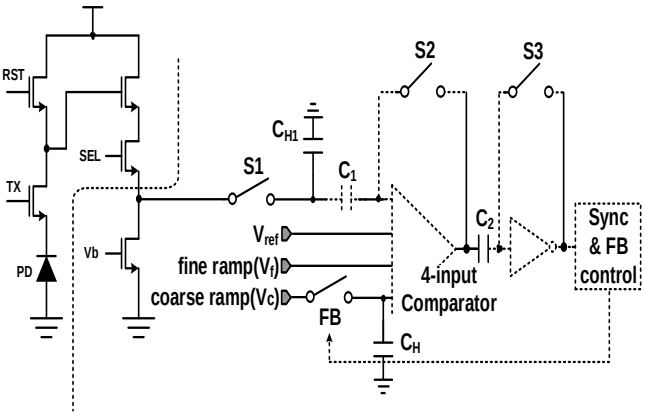


Fig. 2. Circuit diagrm of ADC with a 4-inpuit comparator

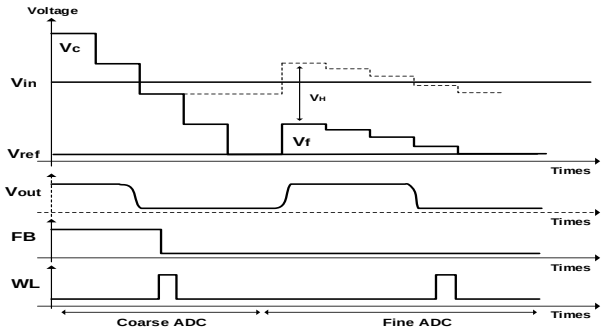
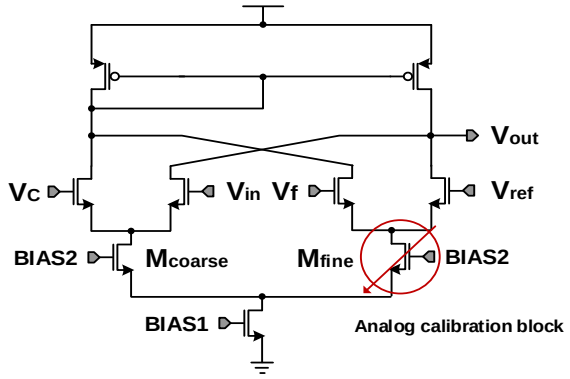
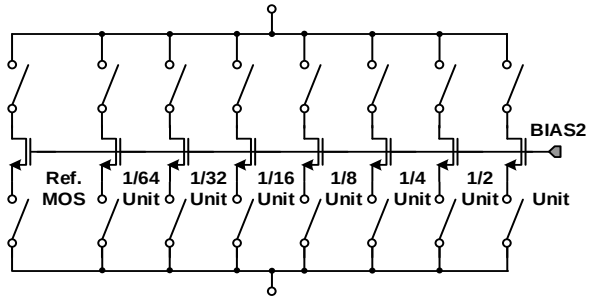


Fig. 3. Timng diagram for coarse ramp and fine ramp



(a)



(b)

Fig. 4. Circuit diagram of the 4-input comparator
(a) the 4-input comparator (b) analog calibration block

https://doi.org/10.17758/EIRAI2.F0418109

Fig.5 shows the flow chart of the proposed self-calibration circuit. The slope correction between the coarse ramp and the fine ramp is performed based on the flow chart above. Fig.6 shows the digital calibration block diagram. First, the initial values configured as the default in the trim SRAM are entered to the analog calibration block for the self-calibration. Then, the analog CDS switch is controlled to convert the lowest fine bit value in the coarse 1 LSB to the digital code and stored to the first memory. Then, the highest fine bit value in the coarse 1 LSB is under the A/D conversion and saved to the second memory. And the two data are subtracted by the subtractor. Here, the difference between the two data causes to change the initial value configured in the trim SRAM depending on whether the value is smaller or larger than the ideal 7-bit fine code value (127). Changing the value in the trim SRAM changes the total amount of the current flowing in the analog calibration circuit and changes the gm value of the M_{Fine}. Repeating such methods finally makes the analog gain between the M_{Coarse} and the M_{Fine} the same. As a result, the CFPN may be corrected due to the difference in the analog gain between the coarse ramp and the fine ramp in the comparator by the mismatching in the process.

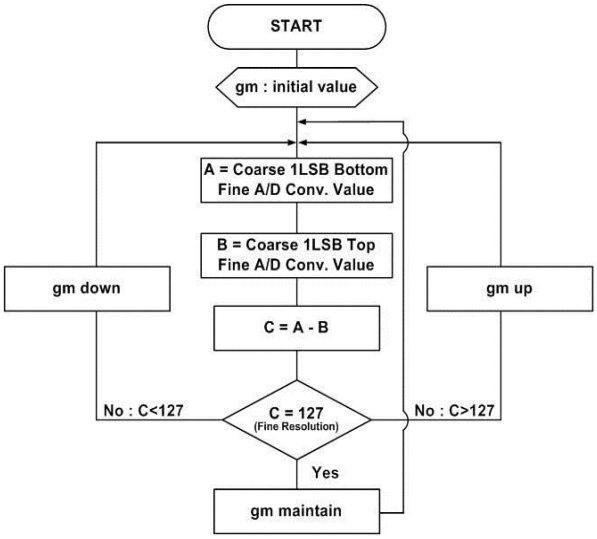


Fig. 5. Flow chart of proposed self-calibration

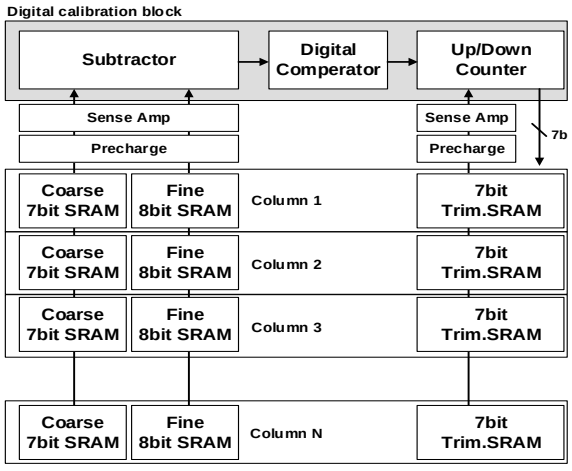


Fig. 6. Digital calibration block diagram

IV. Measurement Result

Fig.7 shows the microphotograph of the CIS manufactured from the 0.13µm 1P4M CIS process. The chip size is 6.5mm x 6.5mm and the pixel array consist of the VGA resolution (640x480). Fig.8 shows the sample image with the VGA grade under the measurement. It meets the frame rates of 120 frames/s at the main clock of 40MHz and the ADC clock of 20MHz. Fig.9 shows the sample images to check the image changes by the self-calibration technique. The analog gain difference between the coarse ramp and the fine ramp is very large on the arbitrary basis for the measurement. Fig.9 (a) shows the sample image prior to the self-calibration. The images prior to the self-calibration show very poor image quality due to the high random noise and the CFPN by the degraded ADC linearity from the analog gain difference between the two ramps. Fig.9 (b) shows the sample images after the self-calibration. The ADC linearity increases owing to the calibration of the analog gain difference between the two ramps after the self-calibration. Therefore, the CFPN and the random noise in the image sensor are significantly decreased and the improved image quality may be achieved.

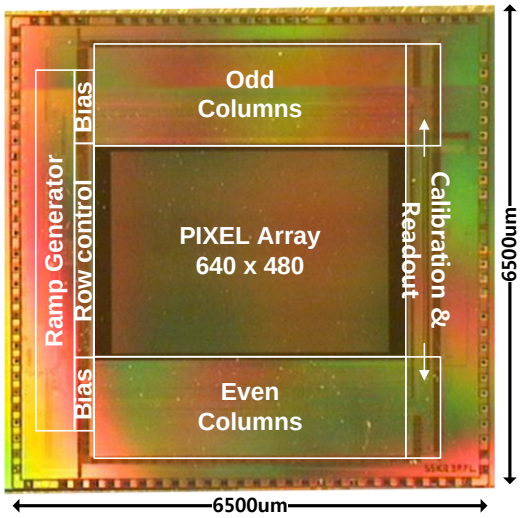


Fig. 7. Photograph of the fabricated CIS

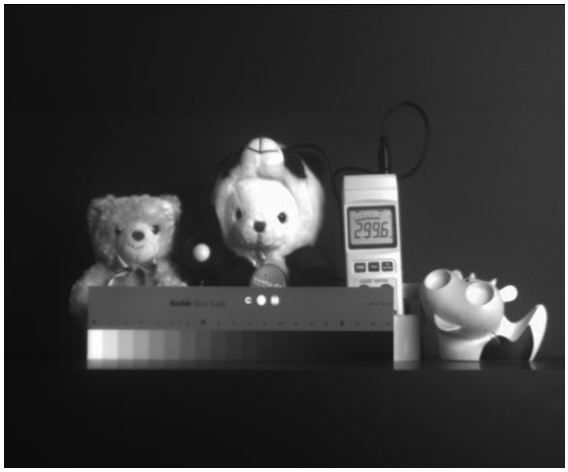
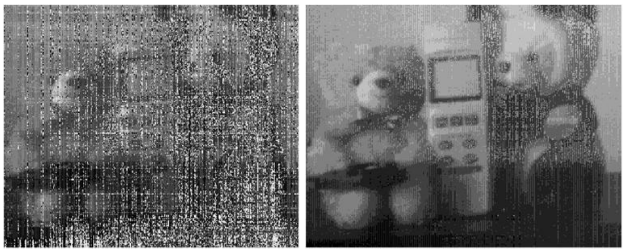


Fig. 8. Measured Image with the proposed CIS chip



(a) (b)

Fig. 9. Measured sample images (a) sample image before self-calibration (b) sample image after self-calibration

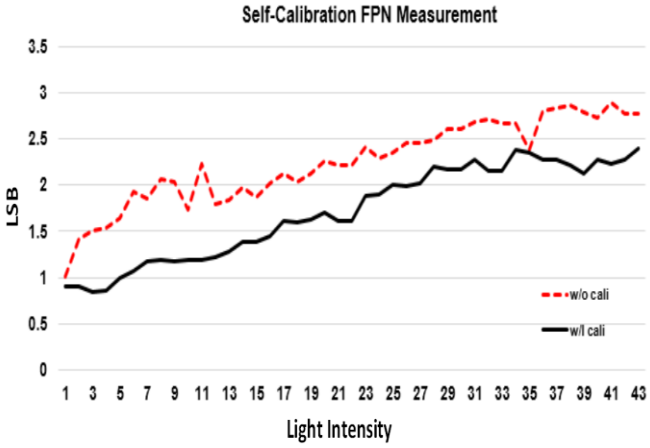


Fig. 10. CFPN of before/after self-calibration

Fig.10 shows the CFPN before and after the self-calibration. The CFPN decreases by about 0.4 LSB after the self-calibration. The final CFPN meets 0.38 LSB in the coarse 7-bit / fine 1-bit (8-bit ADC) data and 5.5 LSB in the coarse 3-bit / fine 5-bit (12-bit ADC) data.

V. Conclusion

A low spurious CMOS image sensor using a hybrid column self-calibration technique was described. A two-step single-slope ADC performed the A/D conversion by separating the coarse bit and fine bit. Thus it was suitable for a high speed CIS. In order to overcome the mismatching problem, however, a 4-input comparator was also discussed. Further, a feedback circuit was designed to calibrate the difference between the coarse ramp and the fine ramp. Therefore, the measured SNR was improved by about 10dB and the CFPN was decreased by more than 0.4 LSB, compared to those of the TS SS ADC without self-calibration. The resolution of the proposed CMOS image sensor was the VGA (640x480) level, and the pixel size was 5.6μm with the 4-TR APS. The conversion time of the designed TS SS ADC was 120 frame/s with 17μs at the main clock of 40MHz. Table I summarizes the performance of the designed CIS. Table II compares the proposed ADC with the previously published works.

TABLE I: Summary of the CIS performance

Process technology	0.13μm 1P4M CIS process
Chip size	6.5μm x 6.5μm
Core size	6mm x 6mm
Number of effective pixel	640 x 480 pixels
Pixel type	Non-shared 4T (pinned-photodiode)
Operating voltage	2.8V(pixel)/2.8V(analog)/1.5(digital)
Frame rate	120 fps (@40Mhz)
ADC resolution	14-bit
P-FPN/C-FPN	0.43 LSB/0.38 LSB (@dark)
Dynamic range	64.6 dB
Power consumption	98 μW/ / column
Full well capacity	23000e^-
Conversion gain	43μV/e^-
Total RN	13.5e^-_{rms}
Figure of Merit	43.9e^-nJ

TABLE II: ADC performance comparison with previous work

Reference	[4]	[5]	[6]	This work
ADC Type	ΔΣ	SAR	Cyclic	TS SS
ADC resolution	>12	14	13	14
Conversion Time [μs]	2.3	1.7	2.3	7.7
1-H Time [μs]	6.85	9.2	6	17
Power consumption [μW]	55	41	300	98
ADC FoM [f J]	15	4.2	84	32

Acknowledgements

This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education, Science and Technology (2015R1D1A1A01058193).

References

[1] T. Sugiki et al., "A 60 mW 10 b CMOS image sensor with column-to-column FPN reduction," in Proc. IEEE ISSCC Dig. Tech. Papers, Feb. 2000,pp. 108-109,450.
https://doi.org/10.1109/ISSCC.2000.839712

[2] S. Lim, J. Cheon, S. Ham, and G. Han, "A new correlated double sampling and single slope ADC circuit for CMOS image sensors," in Proc. Int. SoC Des. Conf., Oct. 2004, pp. 129–131.

[3] M. F. Snoeij et al., "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," IEEE J. Solid-State Circuits, vol. 42, no. 12, Dec. 2007, pp. 2968–2967.
https://doi.org/10.1109/JSSC.2007.908720

[4] Y.-C. Chae, J.-M. Cheon, S.-H. Lim, M.-H. Kwon, K.-S. Yoo, W.-K. Jung, D.-H. Lee, S.-H. Ham and G.-H. Han, "A 2.1 MPixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ΔΣ Architecture," IEEE J. Solid-State Circuits, vol. 46, no. 1, Jan. 2011, pp. 236-247.
https://doi.org/10.1109/JSSC.2010.2085910

[5] J.-H. Kim, W.-K. Jung, S.-H. Lim, Y.-J. Park, W.-H. Choi, Y.-J. Kim, C.-E. Kang, J.-H. Shin, K.-J. Choo, W.-B. Lee, J.-K. Heo, B.-J. Kim, S.-J. Kim, M.-H. Kwon, K.-S. Yoo. J.-H. Seo, S.-H. Ham, C.-Y. Choi and G.-S. Han, "A 14b Extended Counting ADC Implemented in a 24MPixel APS-C CMOS Image Sensorm," in IEEE ISSCC Dig. Tech. Papers, Feb. 2012, pp. 390-391.

[6] K. Kitamura, T. Watabe, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito and N. Egami, "A 33-Megapixel 120-Frames-Per-Second 2.5-Watt CMOS Image Sensor With Column-Parallel Two-Stage Cyclic Analog-to-Digital Converters," IEEE Trans. Electron Device, vol. 59, no. 12, Dec. 2012, pp. 3426-3433
https://doi.org/10.1109/TED.2012.2220364